Shanquan Tian

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Education

Yale University **Sept. 2017 - May 2023**
Ph.D. Candidate, Department of Electrical Engineering
Advisor: Prof. Jakub Szefer

Yale University **Sept. 2017 - May 2020**
M.S., Electrical Engineering and M.Phil, Electrical Engineering

University of Science and Technology of China (USTC) **Sept. 2013 - June 2017**
B.S., Applied Physics

Professional Experience

Google | Software Engineering Intern June 2022 - Aug. 2022
Sunnyvale, California

Alibaba Cloud (U.S.) | Research Intern July 2020 - Aug. 2020
Sunnyvale, California (Remote)
- Project: Vector Processing Acceleration based on RISC-V

CASLAB, Yale University | Research Assistant Sept. 2017 - Present
New Haven, Connecticut

Peer-reviewed Publications

- Ilias Giechaskiel, **Shanquan Tian**, Jakub Szefer. "Cross-VM Covert-and Side-Channel Attacks in Cloud FPGAs" in ACM Transactions on Reconfigurable Technology and Systems (**TRETS**), 2022.
- Ilias Giechaskiel, **Shanquan Tian**, Jakub Szefer. "Cross-VM Information Leaks in FPGA-Accelerated Cloud Environments" in Proceedings of the International Symposium on Hardware Oriented Security and Trust, **HOST**, 2021.
- Shayan Moini, **Shanquan Tian**, Daniel Holcomb, Jakub Szefer, and Russell Tessier. "Power Side-Channel Attacks on BNN Accelerators in Remote FPGAs" in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, **JETCAS**, 2021.
- **Shanquan Tian**, Shayan Moini, Adam Wolnikowski, Daniel Holcomb, Russell Tessier, and Jakub Szefer. "Remote Power Attacks on the Versatile Tensor Accelerator in Multi-Tenant FPGAs" in Proceedings of the International Symposium on Field-Programmable Custom Computing Machines (**FCCM'21**), **Best Paper Candidate**, May 2021.
- **Shanquan Tian**, Ilias Giechaskiel, Wenjie Xiong, and Jakub Szefer. "Cloud FPGA Cartography using PCIe Contention" in Proceedings of the International Symposium on Field-Programmable Custom Computing Machines (**FCCM'21**), May 2021.
- Shayan Moini, **Shanquan Tian**, Jakub Szefer, Daniel Holcomb, and Russell Tessier. "Remote Power Side-Channel Attacks on BNN Accelerators in FPGAs" in Design, Automation and Test in Europe Conference (**DATE'21**), February 2021.
- **Shanquan Tian**, Andrew Krzywosz, Ilias Giechaskiel and Jakub Szefer. " Cloud FPGA Security with RO-Based Primitives" in International Conference on Field-Programmable Technology (**FPT'20**), IEEE, 2020.
- Wen Wang, **Shanquan Tian**, Bernhard Jungk, Nina Bindel, Patrick Longa, and Jakub Szefer, "Parameterized Hardware Accelerators for Lattice-Based Cryptography and Their Application to the HW/SW Co-Design of qTESLA", in Proceedings of the Conference on Cryptographic Hardware and Embedded Systems (**CHES'20**), September 2020.
- **Shanquan Tian**, Wenjie Xiong, Ilias Giechaskiel, Kasper Rasmussen and Jakub Szefer. "Fingerprinting Cloud FPGA Infrastructures" in Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA'20**), ACM, 2020.
- **Shanquan Tian**, Wen Wang and Jakub Szefer. "Merge-Exchange Sort Based Discrete Gaussian Sampler with Fixed Memory Access Pattern" in International Conference on Field-Programmable Technology (**FPT'19**), IEEE, 2019.
- **Shanquan Tian**, and Jakub Szefer. "Temporal Thermal Covert Channels in Cloud FPGAs" in Proceedings of the

ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA'19**), ACM, 2019.

Teaching Experience

Teaching Fellow | Yale University, New Haven, CT, USA — Spring 2022
Cloud FPGA (EENG428)

Teaching Fellow | Yale University, New Haven, CT, USA — Spring 2020 & 2019
Introduction to Computer Engineering (EENG201)

Presentations & Talks

Conference Talks

- "Remote Power Attacks on the Versatile Tensor Accelerator" at FCCM'21, virtual, May 2021
- "Cloud FPGA Cartography using PCIe Contention" at FCCM'21, virtual, May 2021
- "Cloud FPGA Security with RO-Based Primitives" at FPT'20, virtual, December, 2020
- "Fingerprinting Cloud FPGA Infrastructures" at FPGA'20, Seaside, CA, USA, February 2020
- "Merge-Exchange Sort Based Discrete Gaussian Sampler with Fixed Memory Access Pattern" at FPT'19, Tianjin, China, December 2019
- "Temporal Thermal Covert Channels in Cloud FPGAs" at FPGA'19, Seaside, CA, USA, February 2019

Hardware Demo

- "Fingerprinting Cloud FPGA Infrastructures", Hardware Demo at the International Symposium on Hardware Oriented Security and Trust (HOST'20), December 2020

Professional Service

- Reviewer for IEEE Computer Architecture Letters

Skills

- **Programming**: C/C++, Verilog/System Verilog, Python, TensorFlow, PyTorch, Numpy, Chisel, R, SQL, Assembly
- **Tools**: AWS tools, Docker, Kubernetes, Xilinx Vivado/ISE, Quartus, Jupyter Notebook

Selected Honors & Awards

- Conference Travel Grant, FPGA'19 & FPGA'20 — 2019&2020
- Golden Scholarship for Outstanding Student (1st Grade) of USTC — 2015
- National Scholarship (The highest scholarship for Chinese undergraduates) — 2014