Homework 5
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Homework Questions

For this homework, please complete textbook question **5.2** from Chapter 5. Complete the question by writing Verilog code. There are no text or written answers to be submitted for this homework.

You are encouraged to use `iverilog` and `gtkwave` to check your code synthesizes correctly and that it operates as expected.

Homework Time Estimate

To help improve homeworks, please estimate the number of hours used to complete this homework (reading instructions, debugging, etc.). Please round up your estimate to the nearest hour. For the homework, please put your answer as a single integer number of hours in your *git* repository in the file `homeworks/homework-05/TIME-ESTIMATE-HOMEWORK.txt`.

Submission Instructions

Submit your solutions as separate Verilog files. Please all files in your *git* repository in the `homeworks/homework-05/` folder. Please save the files as:

1. Question 5.2, save the file as `exercise_5-2.v`. There is no testbench to be submitted for this question. In total 1 file needs to be submitted for this question.

References