Homework 1
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Homework Questions

For this homework, please complete textbook questions **1.6, 1.7, and 1.8** from Chapter 1. Complete each question by writing Verilog code. There are no text or written answers to be submitted for this homework. For the questions involving writing a testbench, in addition to printing output to the screen, generate a `*.vcd` file where the waveform is saved. Names of the files to be used are discussed below in submission instructions.

You are encouraged to first complete the tutorial *Setting Up Linux Virtual Machine Using VirtualBox*, and use the VM to write and test your code. The modified book examples used in class can be obtained from the `https://bitbucket.org/refezs/eeng428-public-fall2019` repository.

Homework Time Estimate

To help improve homeworks and tutorials, please estimate the number of hours used to complete this homework and the tutorial (reading instructions, setting up tools, debugging, etc.). Please round up your estimate to the nearest hour. Please provide estimate for both the homework and the tutorial. For homework, please put your answer as a single integer number of hours in your *git* repository in the file `homeworks/homework-01/TIME-ESTIMATE-HOMEWORK.txt`. For the tutorial, please put your answer as a single integer number of hours in your *git* repository in the file `homeworks/homework-01/TIME-ESTIMATE-TUTORIAL.txt`.

Submission Instructions

Submit your solutions as separate Verilog files. Please all files in your *git* repository in the `homeworks/homework-01/` folder. Please save the files as:

1. Question 1.6, save the files as `exercise_1-6_serialadder.v`, `exercise_1-6_testbench.v`, and `exercise_1-6_tester.v`. Follow the structure of Figure 1.3 in textbook where the tester and the design under test (serial adder in this case) are both submodules of the testbench module. The waveform generated should be saved as `exercise_1-6_testbench.vcd`, submit the waveform as well. In total 4 files need to be submitted for this question.

2. Question 1.7, save the file as `exercise_1-7_sillyme.v`. In total 1 file needs to be submitted for this question.

3. Question 1.8, save the files as `exercise_1-8_the_ckt.v`, `exercise_1-8_testbench.v`, and `exercise_1-8_tester.v`. Again, follow the structure of Figure 1.3 in textbook. The `exercise_1-8_the_ckt.v` is simply the code provided in textbook already. The waveform generated should be saved as `exercise_1-8_testbench.vcd`, submit the waveform as well. In total 4 files need to be submitted for this question.

References